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This book constitutes the refereed proceedings of the 8th International Conference on High-Performance Computing and Networking, HPCN Europe 2000, held in Amsterdam, The Netherlands, in May 2000. The 52 revised

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full papers presented together with 34 revised posters were carefully reviewed for inclusion in the book. The papers are organized in sections on problem solving environments, metacomputing, load balancing, numerical parallel algorithms, virtual enterprises and virtual laboratories, cooperation coordination, Web-based tools

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for tele-working, monitoring and performance, low-level algorithms, Java in HPCN, cluster computing, data analysis, and applications in a variety of fields.

With globalization in every area of human activity being a key trend of the 1990s, better and faster networks will have an

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increasingly important role and impact in making the 'global village' a reality. The papers collected in this volume highlight the global nature of the activities and the tremendous pace of R&D in the field of communications and networking.

This book constitutes the proceedings of

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the First International Conference on Space Information Network, SINC 2016, held in Kunming, China, in August 2016. The 18 full and 6 short papers presented in this volume were carefully reviewed and selected from 139 submissions. The theme of the conference encompasses new progress and development tendency of the

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space information network and related fields, There were 3 sections in the proceedings of SINC 2016 including the model of space information network and mechanism of high performance networking, theory and method of high speed transmission in space dynamic network, and sparse representation and

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fusion process in space information.

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winning Web site (Computerworld.com),
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Over the past decade, system-on-chip
(SoC) designs have evolved to address the

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ever increasing complexity of applications, fueled by the era of digital convergence. Improvements in process technology have effectively shrunk board-level components so they can be integrated on a single chip. New on-chip communication architectures have been designed to support all inter-component

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communication in a SoC design. These communication architecture fabrics have a critical impact on the power consumption, performance, cost and design cycle time of modern SoC designs. As application complexity strains the communication backbone of SoC designs, academic and industrial R&D efforts and dollars are

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increasingly focused on communication architecture design. On-Chip Communication Architectures is a comprehensive reference on concepts, research and trends in on-chip communication architecture design. It will provide readers with a comprehensive survey, not available elsewhere, of all

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current standards for on-chip communication architectures. A definitive guide to on-chip communication architectures, explaining key concepts, surveying research efforts and predicting future trends Detailed analysis of all popular standards for on-chip communication architectures

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Comprehensive survey of all research on communication architectures, covering a wide range of topics relevant to this area, spanning the past several years, and up to date with the most current research efforts. Future trends that will have a significant impact on research and design of communication architectures over the next

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several years

A tutorial providing a comprehensive introduction to LAN and MAN technology and standards, combining original material and reprinted articles in the following organization: local area networks, metropolitan area networks, the network

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interface, LAN and MAN performance,
internetworking, glossary, list

A handy source for practicing engineers
and researchers, this book offers collected
examples of successful performance
evaluation of high speed
telecommunications switching fabrics

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such as ATM networks and high speed interconnection technology for computers. It emphasizes the performance evaluation of such switches as they apply to predicting a proposed system's performance through the use of statistical models -- a cost-saving way for communications engineers to test the

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design of a system without having to
construct it.

This book constitutes the refereed
proceedings of the 26th International
Conference on Architecture of Computing
Systems, ARCS 2013, held in Prague,
Czech Republic, in February 2013. The 29

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papers presented were carefully reviewed and selected from 73 submissions. The topics covered are computer architecture topics such as multi-cores, memory systems, and parallel computing, adaptive system architectures such as reconfigurable systems in hardware and software, customization and application

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specific accelerators in heterogeneous architectures, organic and autonomic computing including both theoretical and practical results on self-organization, self-configuration, self-optimization, self-healing, and self-protection techniques, operating systems including but not limited to scheduling, memory

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